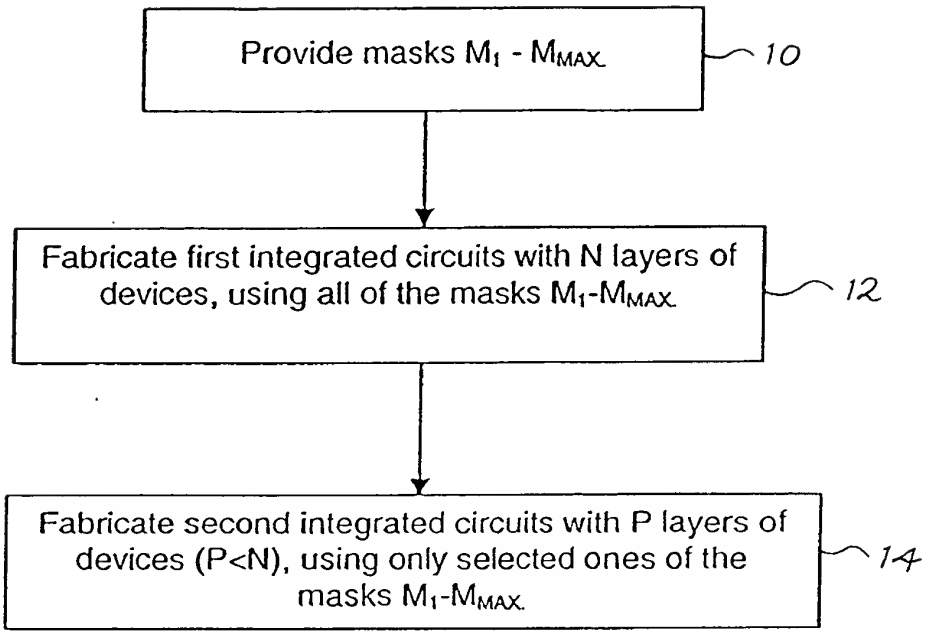

Provide masks M_1 - M_{MAX}
10
Fabricate first integrated circuits with N layers of devices, using all of the masks M_1-M_{MAX}
12
Fabricate second integrated circuits with P layers of devices (P<N), using only selected ones of the masks M_1-M_{MAX}
14

Fig. 1

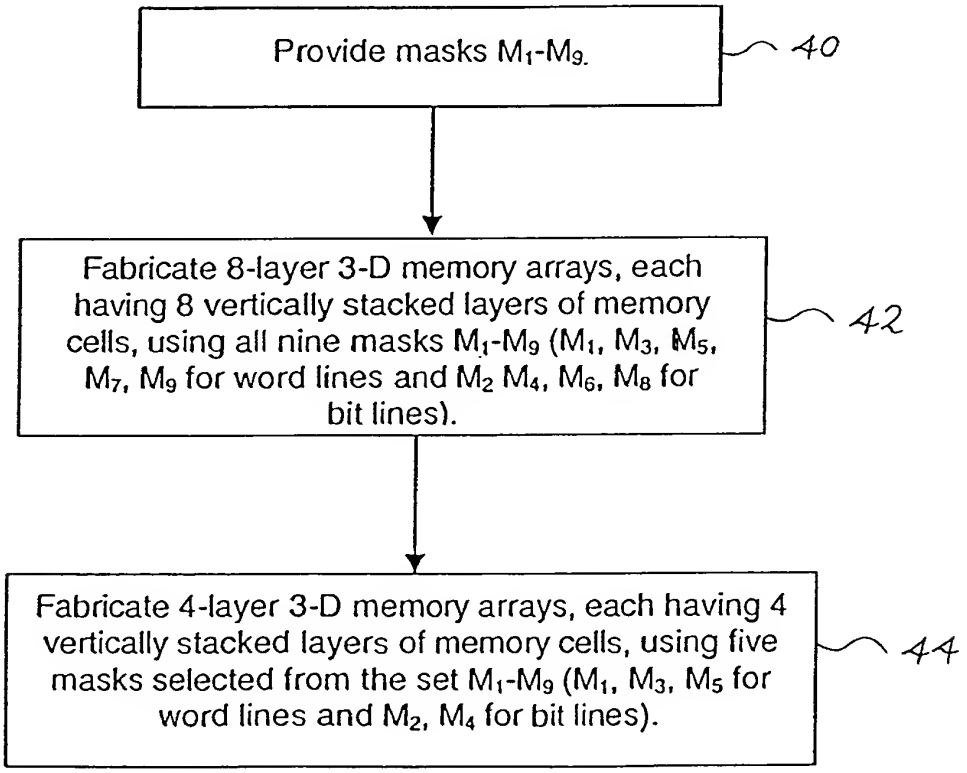
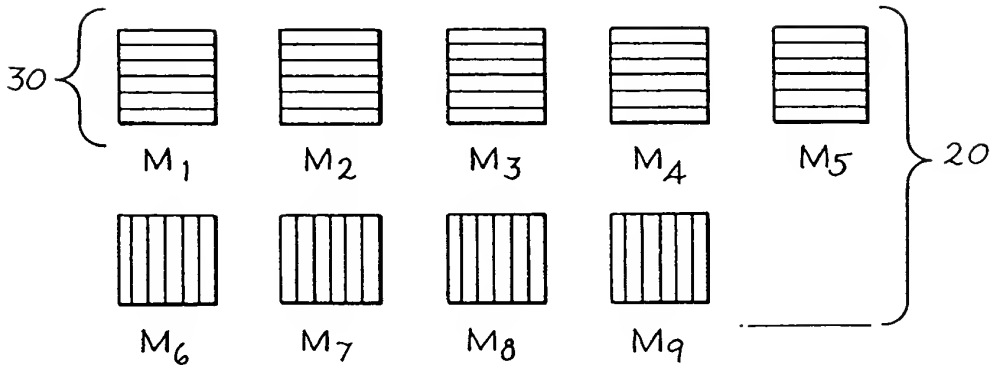

Provide masks M_1-M_9.
40
Fabricate 8-layer 3-D memory arrays, each having 8 vertically stacked layers of memory cells, using all nine masks M_1-M_9 (M_1, M_3, M_5, M_7, M_9 for word lines and M_2 M_4, M_6, M_8 for bit lines).
42
Fabricate 4-layer 3-D memory arrays, each having 4 vertically stacked layers of memory cells, using five masks selected from the set M_1-M_9 (M_1, M_3, M_5 for word lines and M_2, M_4 for bit lines).
44

Fig. 2

Fig. 3



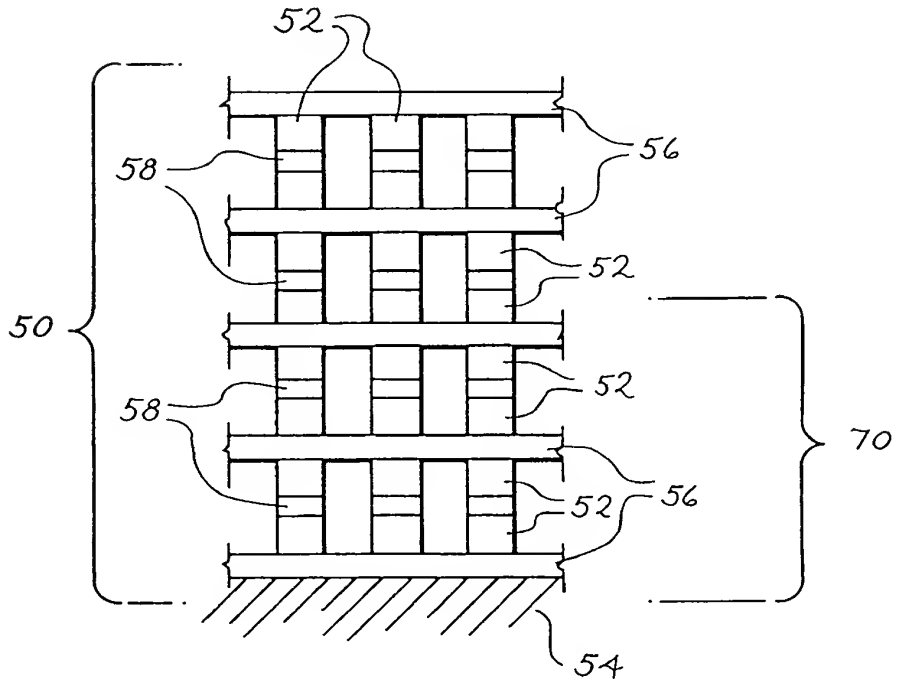


Fig. 4

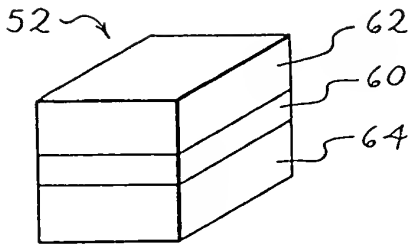

52
62
60
64

Fig. 5

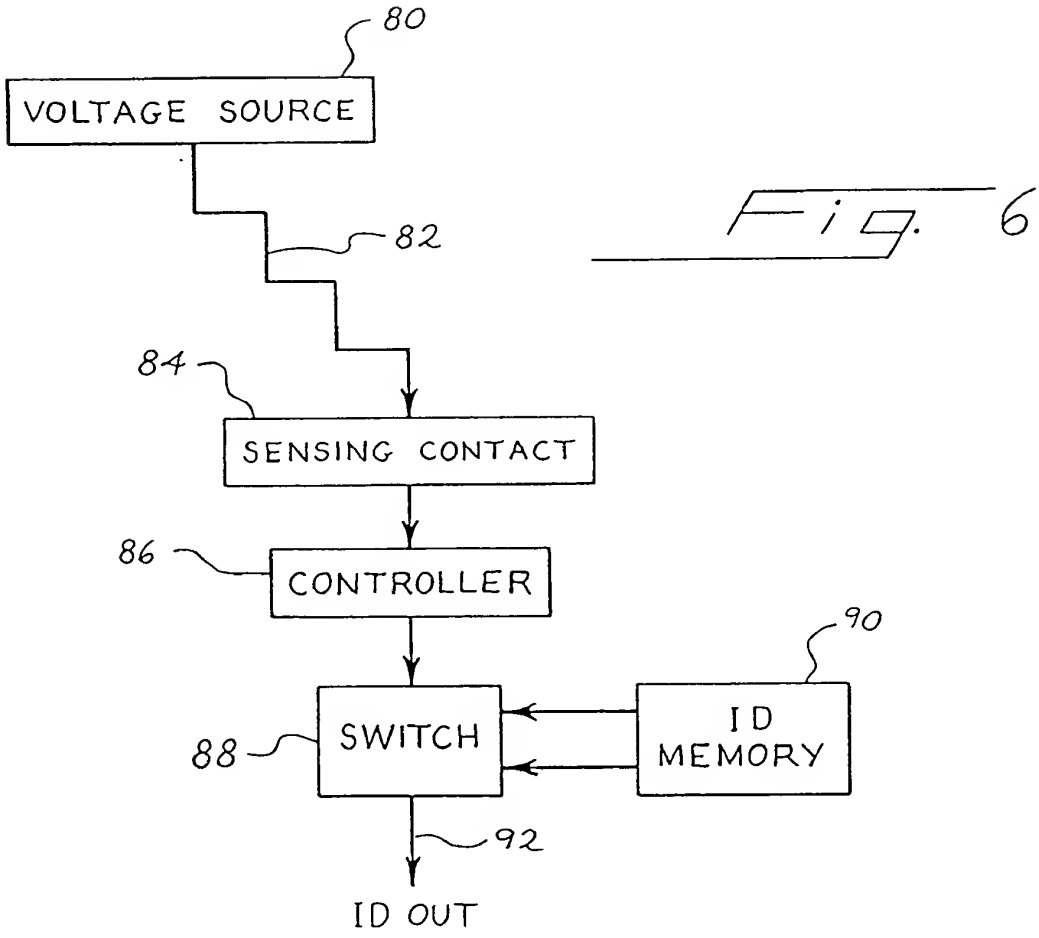

80
VOLTAGE SOURCE
82
84
SENSING CONTACT
86
CONTROLLER
90
88
SWITCH
ID MEMORY
92
ID OUT

Fig. 6

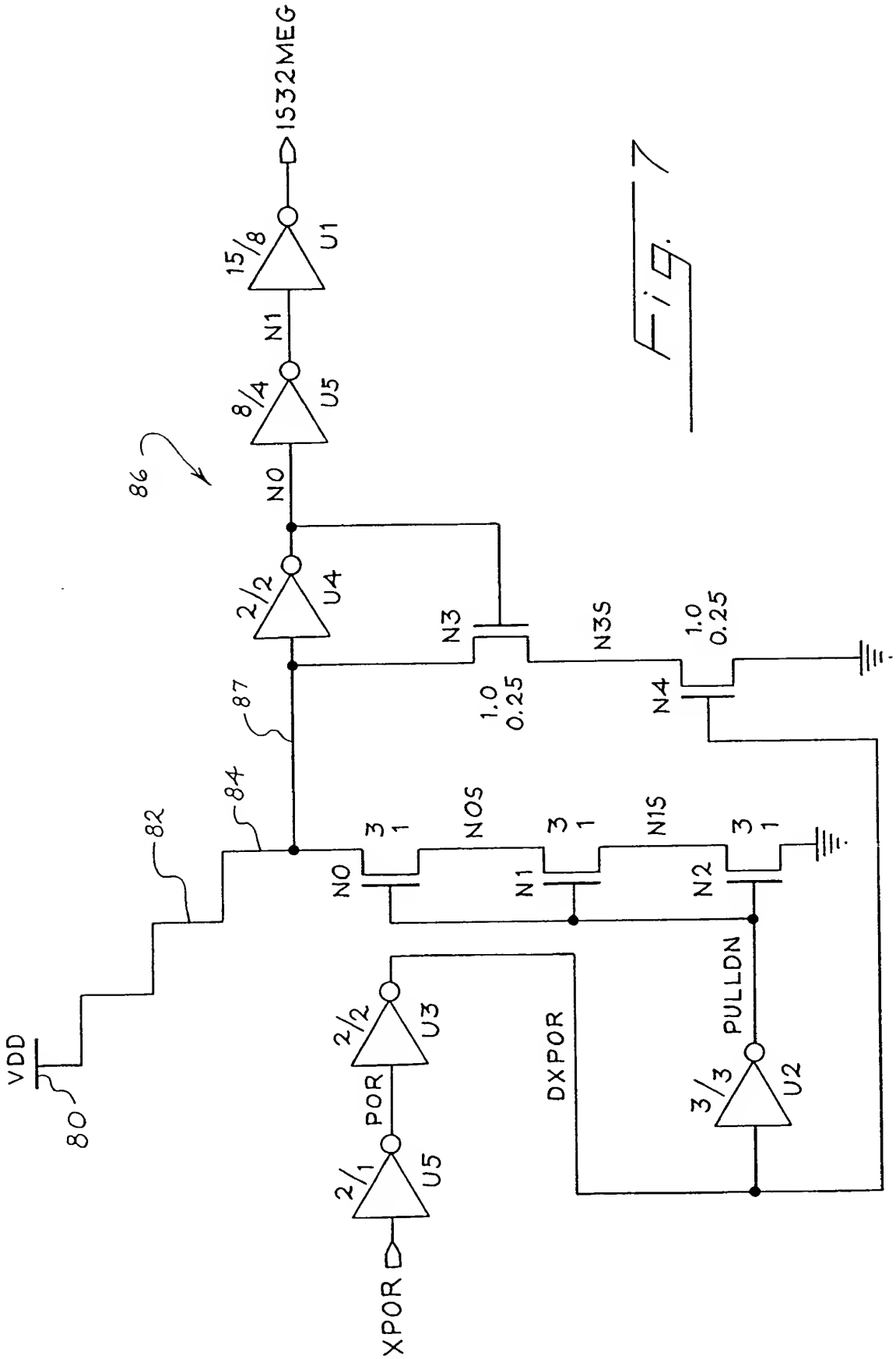

1532MEG
15/8
U1
N1
8/4
U5
86
N0
2/2
U4
N3
1.0
0.25
N3S
1.0
0.25
N4
87
84
82
3
1
NOS
3
1
N1S
3
1
N0
N1
N2
2/2
U3
POR
2/1
U5
XPOR
DXPOR
PULLDN
3/3
U2
VDD
80

Fig. 7

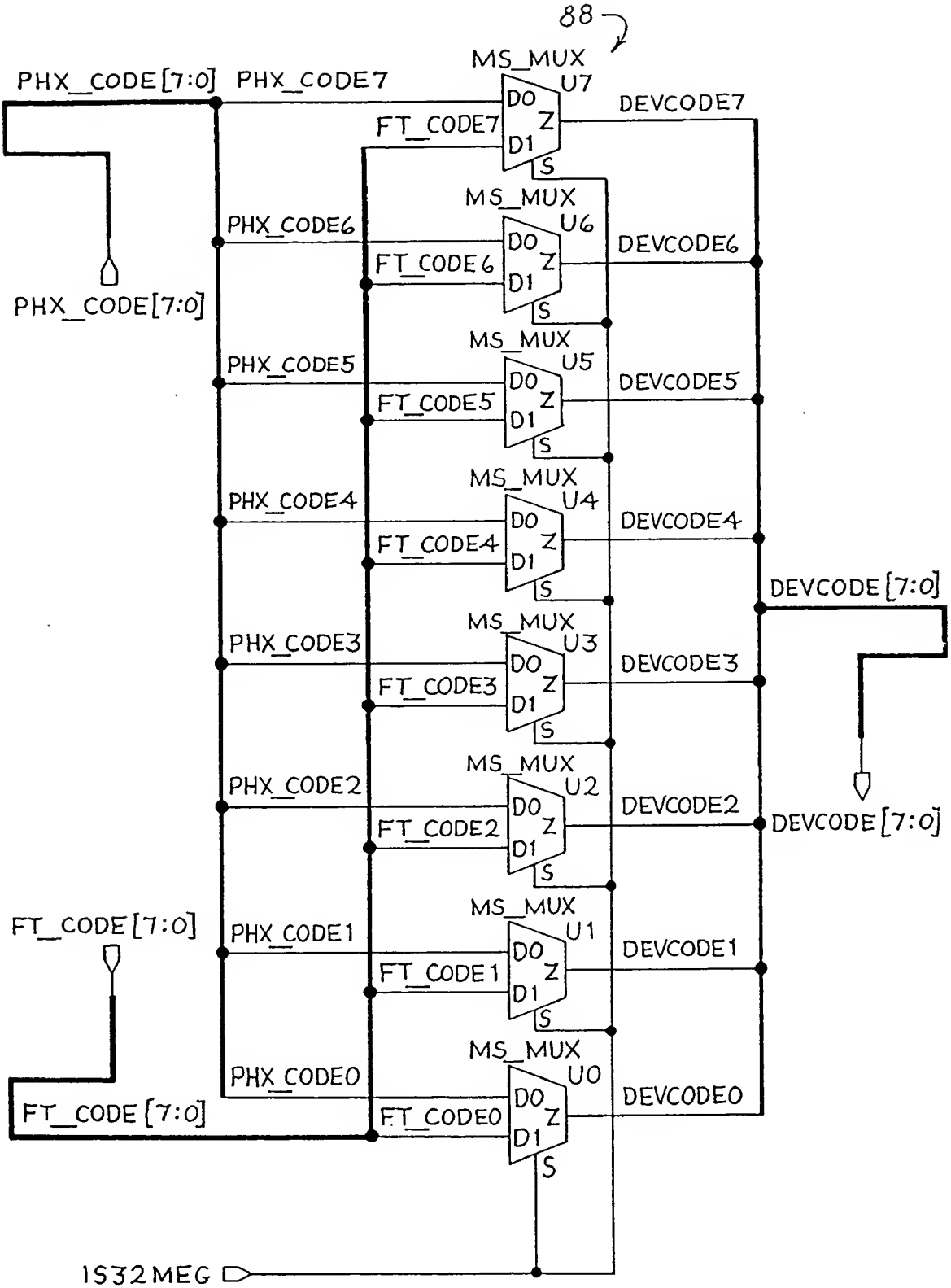

88
MS_MUX
U7
U6
U5
U4
U3
U2
U1
U0
DO
D1
Z
S
PHX_CODE[7:0]
PHX_CODE7
PHX_CODE6
PHX_CODE5
PHX_CODE4
PHX_CODE3
PHX_CODE2
PHX_CODE1
PHX_CODE0
FT_CODE[7:0]
FT_CODE7
FT_CODE6
FT_CODE5
FT_CODE4
FT_CODE3
FT_CODE2
FT_CODE1
FT_CODE0
DEVCODE7
DEVCODE6
DEVCODE5
DEVCODE4
DEVCODE3
DEVCODE2
DEVCODE1
DEVCODE0
DEVCODE[7:0]
1S32MEG

Fig. 8

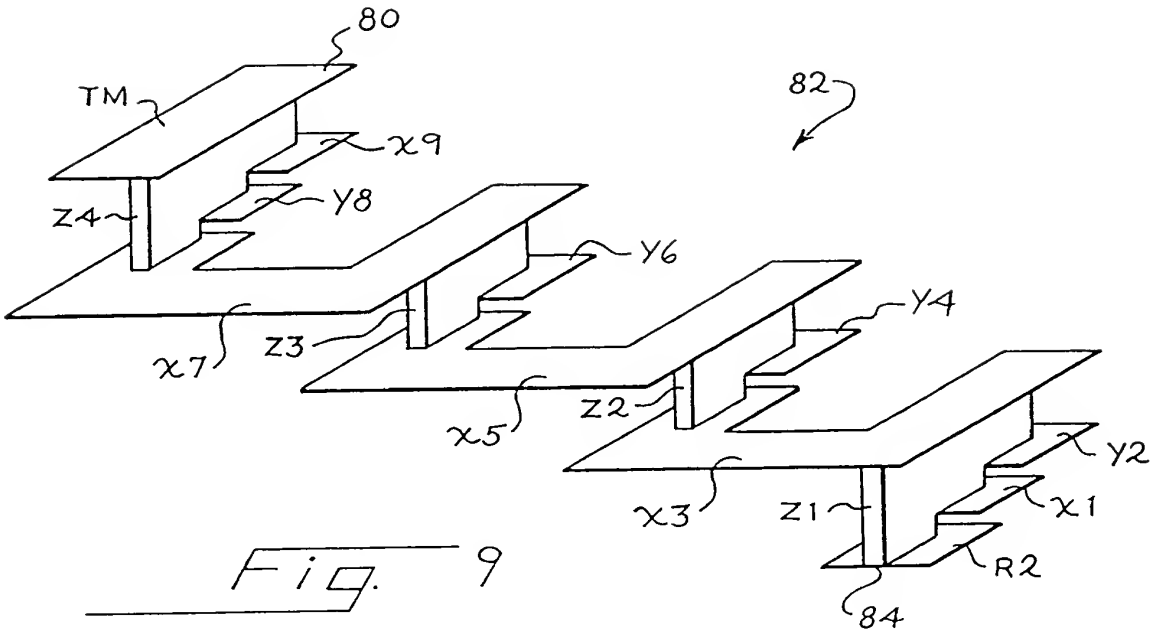
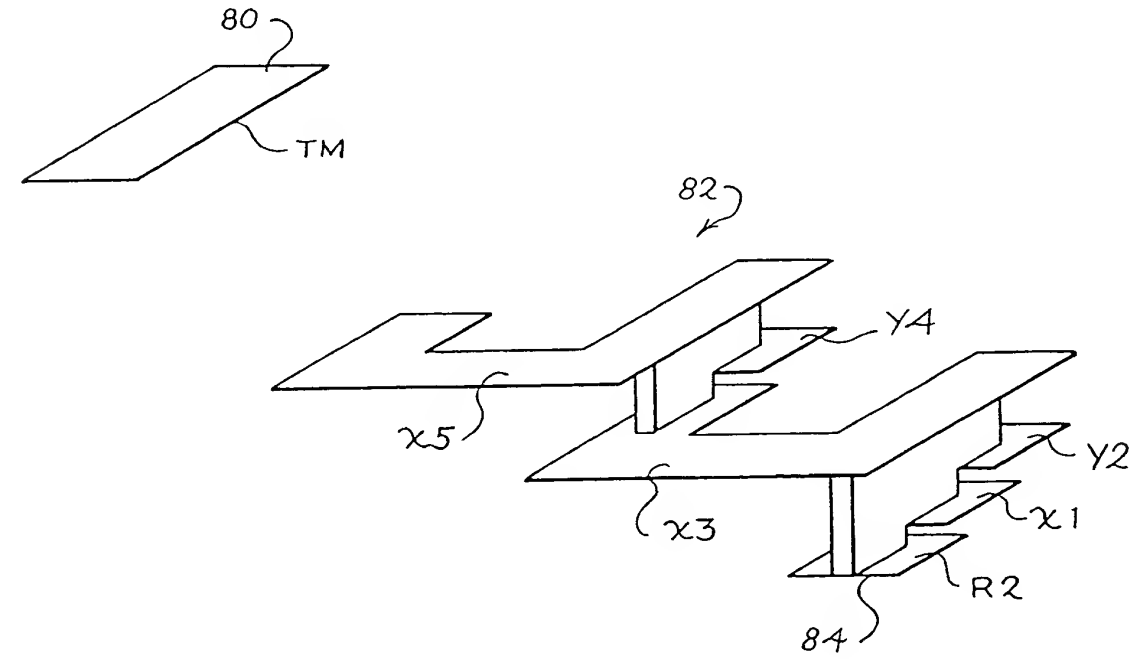

80
TM
82
X9
Y8
Z4
Y6
Y4
X7
Z3
X5
Z2
Y2
X3
Z1
X1
R2
84

Fig. 9

Fig. 10


80
TM
82
Y4
X5
Y2
X3
X1
R2
84

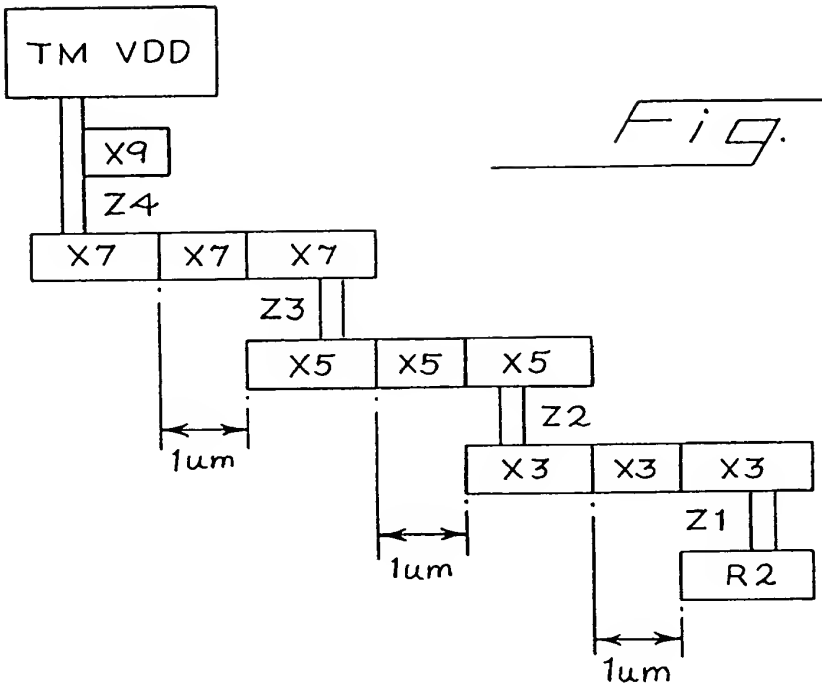


Fig. 11

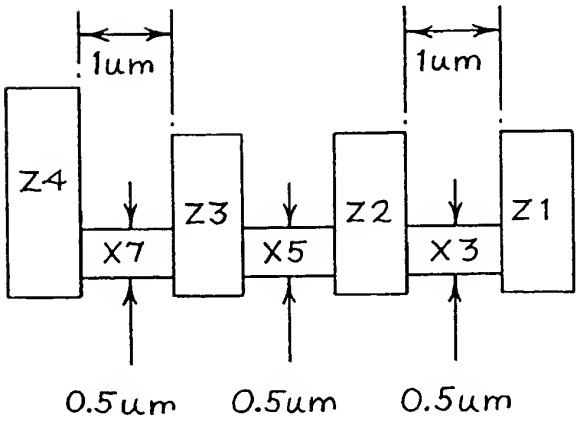


Fig. 12

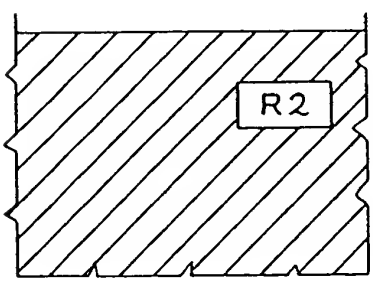


Fig. 13

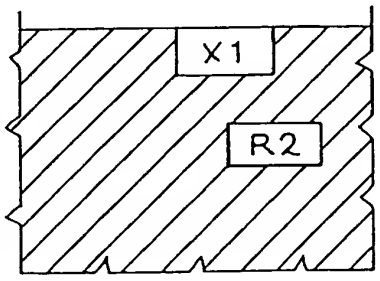


Fig. 14

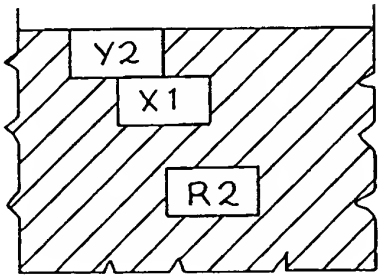


Fig. 15

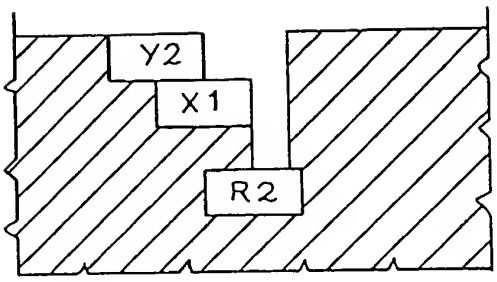


Fig. 16

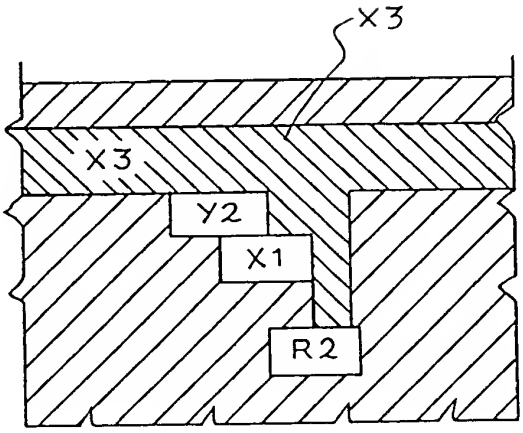


Fig. 17

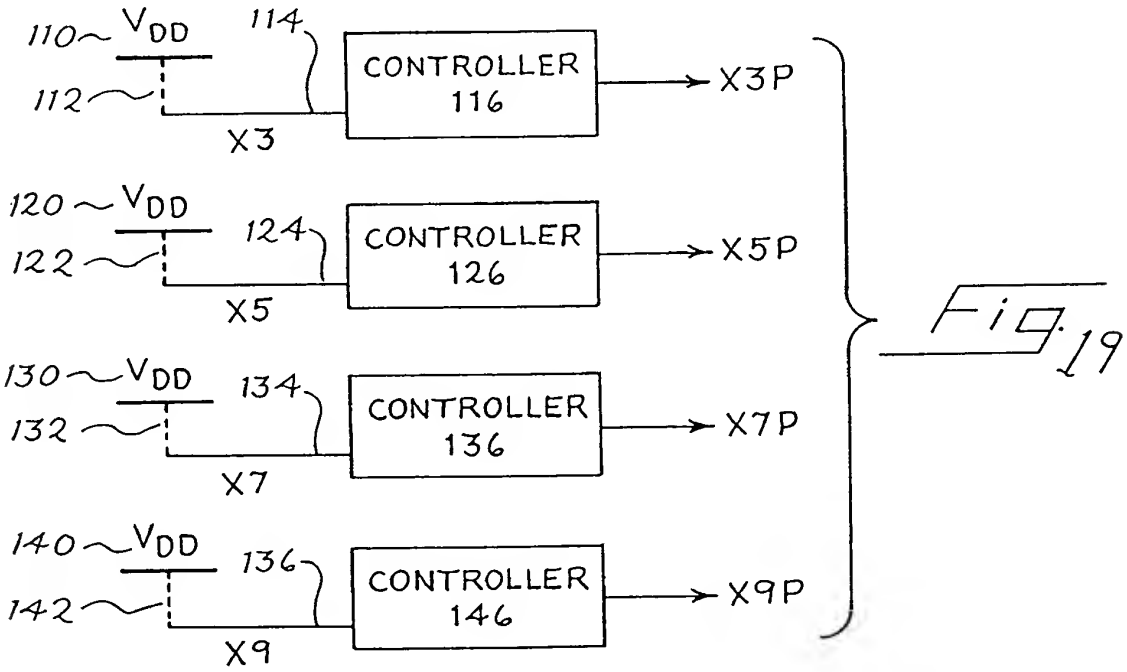


Fig. 19

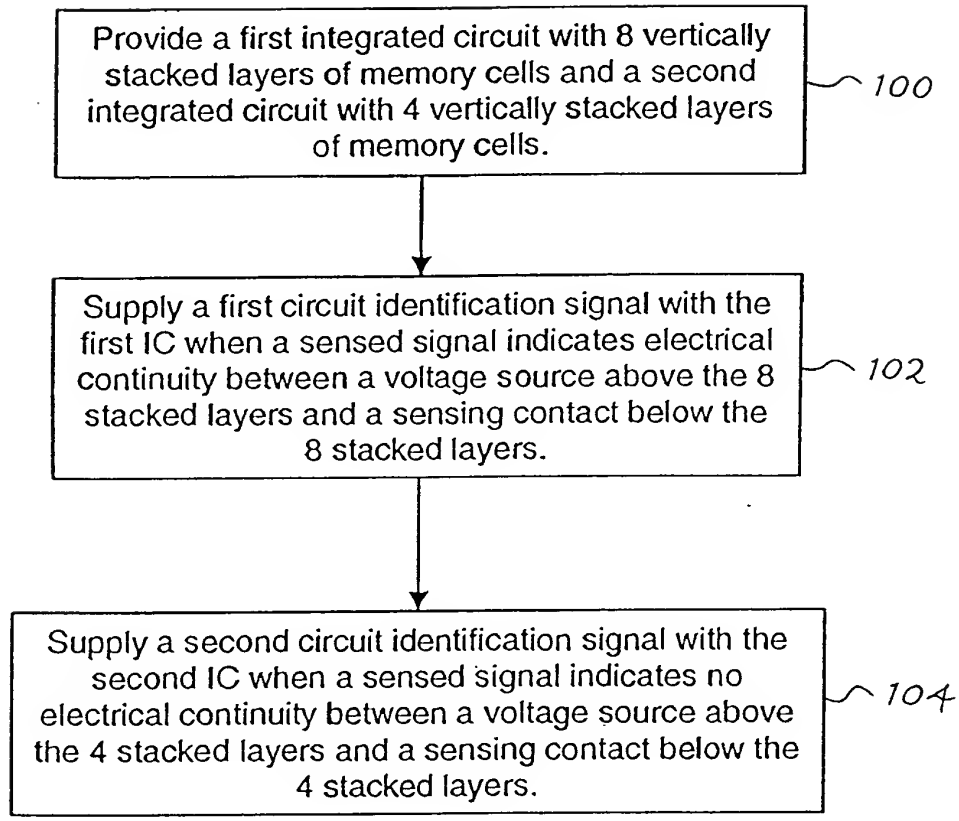

Provide a first integrated circuit with 8 vertically stacked layers of memory cells and a second integrated circuit with 4 vertically stacked layers of memory cells.
100
Supply a first circuit identification signal with the first IC when a sensed signal indicates electrical continuity between a voltage source above the 8 stacked layers and a sensing contact below the 8 stacked layers.
102
Supply a second circuit identification signal with the second IC when a sensed signal indicates no electrical continuity between a voltage source above the 4 stacked layers and a sensing contact below the 4 stacked layers.
104

Fig. 18

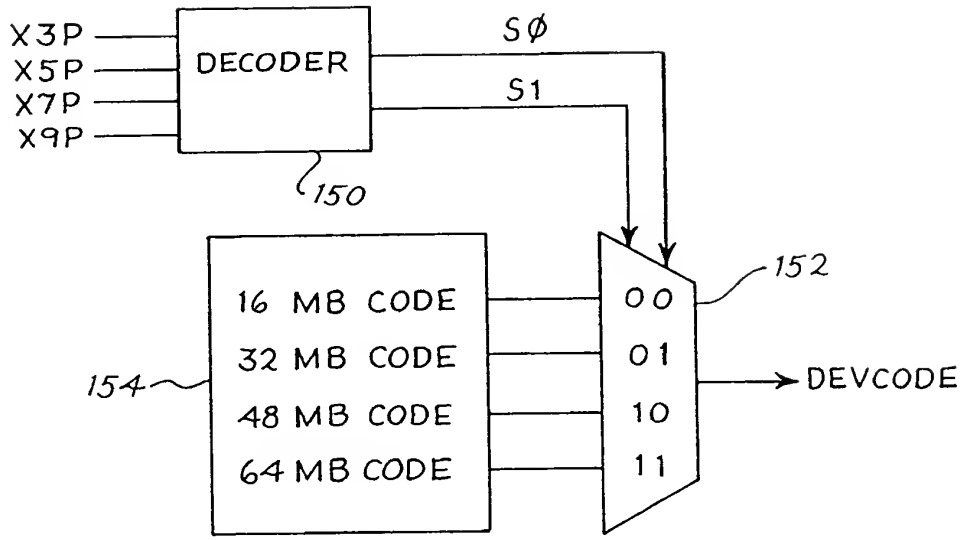


Fig. 20

X3P	X5P	X7P	X9P	S1	SØ
1	0	0	0	0	0
X	1	0	0	0	1
X	X	1	0	1	0
X	X	X	1	1	1

Fig. 21